WHAT IS CLAIMED IS:

1. An oscillation circuit comprising a plurality of constant current supplies for outputting a constant current according to a voltage supplied from a control current terminal, and a plurality of switching elements which are charged or discharged by the constant current outputted from the constant current supplies and are turned on or off when exceeding a predetermined threshold voltage, wherein the voltage from the control current terminal is changed to change a time required until the switching elements are charged or discharged to the threshold voltage, thereby changing an oscillation cycle, said oscillation circuit further including:

restriction elements for restricting a charging target voltage or a discharging target voltage at nodes between the constant current supplies and the switching elements to a constant value.

2. An oscillation circuit as defined in Claim 1, wherein the restriction elements comprise NMOS transistors or PMOS transistors.

3. An oscillation circuit as defined in Claim 1, wherein the restriction elements comprise at least one resistor.

4. An oscillation circuit comprising:

a first delay circuit in which a drain of a PMOS transistor MP1 having a current control terminal as its gate input and a power supply as its source input is connected to a drain of an NMOS transistor MN4, a gate input of the NMOS transistor MN4 is connected to the power supply, a source of the NMOS transistor MN4 and a drain of the NMOS transistor MN1 are connected at a node A1, and a source of the NMOS transistor MN1 is connected to a GND, said first delay circuit having a gate input of the NMOS transistor MN1 as its input and the node A1 as its output;

a second delay circuit in which a drain of a PMOS transistor MP2 having the current control terminal as its gate input and the power supply as its source input is connected to a drain of an NMOS transistor MN5, a gate input of the NMOS transistor MN5 is connected to the power supply, a source of the NMOS transistor MN5 and a drain of the NMOS transistor MN2 are connected at a node A2, and a source of the NMOS transistor MN2 is connected to a GND, said second delay circuit having a gate input of the NMOS transistor MN2 as its input and the node A2 as its output;

a third delay circuit in which a drain of a PMOS transistor MN3 having the current control terminal as its gate input and the power supply as its source input is connected to a drain of an NMOS transistor MN6, a gate input of the NMOS transistor MN6 is connected to the power supply, a source of the NMOS transistor MN6 and the drain of the NMOS transistor MN3 are connected at a node A3, and a source of the NMOS transistor MN3 is connected to

a GND, said third delay circuit having a gate input of the NMOS transistor MN3 as its input and the node A3 as its output; and

said first to third delay circuits being cascade-connected so that the output A1 of the first delay circuit is connected to the input of the second delay circuit, the output A2 of the second delay circuit is connected to the input of the third delay circuit, and the output A3 of the third delay circuit is connected to the input of the first delay circuit.

5. An oscillation circuit as defined in Claim 4, wherein the gate inputs of the NMOS transistors MN4, MN5, and MN6 are fixed to an arbitrary constant voltage.

6. An oscillation circuit comprising:

a first delay circuit in which a drain of an NMOS transistor MN1 having a current control terminal as its gate input and a GND as its source input is connected to a drain of a PMOS transistor MP4, a gate input of the PMOS transistor MP4 is connected to the GND, a source of the PMOS transistor MP4 and a drain of the PMOS transistor MP1 are connected at a node A1, and a source of the PMOS transistor MP1 is connected to a power supply, said first delay circuit having a gate input of the PMOS transistor MP1 as its input and the node A1 as its output;

a second delay circuit in which a drain of an NMOS transistor MN2 having the current control terminal as its gate input and the

GND as its source input is connected to a drain of a PMOS transistor MP5, a gate input of the PMOS transistor MP5 is connected to the GND, a source of the PMOS transistor MP5 and a drain of the PMOS transistor MP2 are connected at a node A2, and a source of the PMOS transistor MP2 is connected to a power supply, said second delay circuit having a gate input of the PMOS transistor MP2 as its input and the node A2 as its output;

a third delay circuit in which a drain of an NMOS transistor MN3 having the current control terminal as its gate input and the GND as its source input is connected to a drain of a PMOS transistor MP6, a gate input of the PMOS transistor MP6 is connected to the GND, a source of the PMOS transistor MP6 and the drain of the PMOS transistor MP3 are connected at a node A3, and a source of the PMOS transistor MP3 is connected to a power supply, said third delay circuit having a gate input of the PMOS transistor MP3 as its input and the node A3 as its output; and

said first to third delay circuits being cascade-connected so that the output A1 of the first delay circuit is connected to the input of the second delay circuit, the output A2 of the second delay circuit is connected to the input of the third delay circuit, and the output A3 of the third delay circuit is connected to the input of the first delay circuit.

7. An oscillation circuit as defined in Claim 6, wherein the gate inputs of the PMOS transistors MP4, MP5, and MP6 are an

arbitrary constant voltage.

8. An oscillation circuit comprising:

a first delay circuit in which a drain of a PMOS transistor MP1 having a current control terminal as its gate input and a power supply as its source input is connected to a drain of an NMOS transistor MN13, a drain of a PMOS transistor MP2 having the current control terminal as its gate input and the power supply as its source input is connected to a drain of an NMOS transistor MN14, gate inputs of the NMOS transistors MN13 and MN14 are connected to the power supply, a source of the NMOS transistor MN13 and drains of NMOS transistors MN1 and MN2 are connected at a node A1, and a source of the NMOS transistor MN14 and drains of NMOS transistor MN4 and MN3 are connected at a node A2, and the sources of the NMOS transistors MN1, MN2, MN3, and MN4 are connected to a GND, said first delay circuit having a gate input of the NMOS transistor MN1 as its positive side input, the gate input of the NMOS transistor MN4 as its negative side input, the node A1 as its negative side output, and the node A2 as its positive side output;

a second delay circuit in which a drain of a PMOS transistor MP3 having the current control terminal as its gate input and the power supply as its source input is connected to a drain of an NMOS transistor MN15, a drain of a PMOS transistor MP4 having the current control terminal as its gate input and the power supply

as its source input is connected to a drain of an NMOS transistor MN16, gate inputs of the NMOS transistors MN15 and MN16 are connected to the power supply, a source of the NMOS transistor MN15 and drains of NMOS transistors MN5 and MN6 are connected at a node A3, a source of the NMOS transistor MN16 and drains of NMOS transistor MN7 and MN8 are connected at a node A4, and the sources of the NMOS transistors MN5, MN6, MN7, and MN8 are connected to a GND, said second delay circuit having the gate input of the NMOS transistor MN5 as its positive side input, the gate input of the NMOS transistor MN8 as its negative side input, the node A3 as its negative side output, and the node A4 as its positive side output;

a third delay circuit in which a drain of a PMOS transistor MP5 having the current control terminal as its gate input and the power supply as its source input is connected to a drain of an NMOS transistor MN17, a drain of a PMOS transistor MP6 having the current control terminal as its gate input and the power supply as its source input is connected to a drain of an NMOS transistor MN18, gate inputs of the NMOS transistors MN17 and MN18 are connected to the power supply, a source of the NMOS transistor MN17 and drains of NMOS transistors MN9 and MN10 are connected at a node A5, a source of the NMOS transistor MN18 and drains of NMOS transistor MN11 and MN12 are connected at a node A6, and the sources of the NMOS transistors MN9, MN10, MN11, and MN12 are connected to a GND, said third delay circuit having the gate

input of the NMOS transistor MN9 as its positive side input, the gate input of the NMOS transistor MN12 as its negative side input, the node A5 as its negative side output, and the node A6 as its positive side output; and

said first to third delay circuits being cascade-connected such that

the negative side output A1 of the first delay circuit is connected to the positive side input of the second delay circuit, and the positive side output A2 of the first delay circuit is connected to the negative side input of the second delay circuit,

the negative side output A3 of the second delay circuit is connected to the positive side input of the third delay circuit, and the positive side output A4 of the second delay circuit is connected to the negative side input of the third delay circuit, and

the negative side output A5 of the third delay circuit is connected to the positive side input of the first delay circuit, and the positive side output A6 of the third delay circuit is connected to the negative side input of the first delay circuit.

9. An oscillation circuit as defined in Claim 8, wherein the gate inputs of the NMOS transistors MN13, MN14, MN15, MN16, MN17, and MN18 are an arbitrary constant voltage.

10. An oscillation circuit as defined in any of Claims 4 to 9,

wherein the number of the delay circuits to be cascade-connected is N (N: integer equal to or larger than 2).